Application Note

INTERFACING THE EP7312 WITH SDRAM

1. INTRODUCTION

The focus of this note is to aid product developers in successfully creating an EP7312 design that utilizes SDRAM. It does not cover the software configuration or internal operation of the controller. For information on enabling and using the SDRAM controller of the EP7312, please read the *EP73xx User's Guide (*DS508).

The SDRAM controller on the EP7312 conforms to the JEDEC No. 21-C standard for power-up and initialization. The User's Guide describes the power-up sequence required. The model for a typical SDRAM device used in developing this controller was derived from NEC's device specifications.

A list of SDRAM parts verified to function with the EP7312 is located in Section 5.3 on page 4. There are many components outside this recommended list that should operate well with this controller. You may use this document along with the *EP7312 Data Sheet* and the data sheet for the desired device in determining compatibility.

2. SDRAM SIGNALS

The EP7312 is capable of generating the appropriate signals necessary to attach up to four banks of SDRAM across a 32-bit data bus. These signals are described in the following section.

2.1 SDCLK/SDCKE

SDRAM uses a synchronous interface. SDCLK is the clock which all SDRAM signals are referenced to. The SDCLK output of the EP7312 is fed to the clock input of each SDRAM chip. The SDCKE signal complements the clock by providing an inhibit signal to the SDRAM device. For normal operation, this will remain high at least for the duration of any valid bus cycle. It is driven low when the EP7312 is put into suspend mode in order to enable the auto-refresh feature of the SDRAM device.

2.2 RAS/CAS

It is well documented that SDRAM is a matrix, (row, column) whereby each data segment has a two coordinates, thus two addresses. CAS and RAS will assert to indicate that the corresponding column or row address is present on the address bus. RAS and CAS are also instrumental in issuing non-transaction commands to the SDRAM devices.

2.3 Address / Bank Selects

The general purpose address bus of the EP7312 is shared with the SDRAM address bus. Pins A27-A15 become SDRAM signals A0-A12 respectively, and A13-A14 become bank selects BA1 and BA0. Because many peripherals use chip selects and a small subset of the address space provided, the pins on which the SDRAM address is applied start at the most significant end of the bus and go down. This topology more evenly distributes bus loading across all of the address pins. If you follow this guideline when you lay out the processor schematic, SDRAM accesses will occur in their proper addresses.

Bank selects are a critical part of the address configuration. BA0 and BA1 refer to bank select 0 and bank select 1 respectively. All SDRAM chips

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are internally divided into either two or four banks. Banks are selected as a binary combination of BA0 and BA1. It is important to understand that there is no functional difference between any of the banks in an SDRAM device. Should BA0 and BA1 be accidentally reversed in the board layout of a system that utilizes both, the SDRAM will still function properly. For systems that use only two banks, BA0 (A14) must be routed to the proper bank select input.

2.4 Data

SDRAMs may be connected to the EP7312 in either a 16-bit or 32-bit fashion. In 16-bit mode, a single 16-bit wide device should be connected to data bus signals D0-D15. For 32-bit mode, either one 32-bit device or two 16-bit devices, side by side, should be attached to D0-D31. Data will only be present after both RAS and CAS (and respective addresses) have been presented on the bus, and CAS latency has expired. Data is transferred across the bus in standard form, i.e. data will be present on the bus in word or half-word format just as it would in a FLASH or SRAM access of the same width.

SDRAM devices can provide an adjustable CAS latency. 'CAS latency' refers to the number of clocks after the READ assertion that data will be available on the bus. Some SDRAM devices support CAS latencies of 1-3 clocks. Our controller allows for latencies of 2-3 only. All SDRAM devices support longer latencies. Please refer to the *EP7312 User's Manual* for information on setting the latency.

2.5 Byte Enable

Data is accessed simultaneously in 8-, 16-, or 32-bit groupings by means of the byte enable signals. SDQM[0-3] are mask bits for the lowest byte through the highest byte, respectively, for SDRAM devices on the data bus. The SDQM signals allow for individual bytes to be written to regardless of the physical SDRAM bus width.

All SDRAM devices require byte enables. A 16-bit access on a 16-bit wide device will require the assertion of SDQM[0-1]. This happens automatically, depending on the nature of the bus access and the device used. The examples on the following pages illustrates how these are used in various SDRAM design implementations.

3. BUS ACCESSES

3.1 Read/Write

The SDRAM controller on the EP7312 always performs a quad word burst when reading or writing regardless of the data type being accessed. This causes a small drop in performance when performing random accesses. Burst accesses provide higher throughput on the SDRAM bus when sequential accesses are performed. Combined with the internal cache, burst transfers overcome the performance penalties of small memory accesses.

3.2 Precharge

The precharge command is used primarily to deactivate an "open" row in a particular bank of SDRAM. Once the controller issues a precharge to a particular bank, subsequent accesses cannot be made until a time specified by the SDRAM device. The SDRAM device will then enter an idle state and require activation before another access can be made. The interval used by the EP7312 SDRAM controller was chosen to be long enough to support SDRAM devices from different manufacturers and families of products.

3.3 Mode Register Command

The load mode register command configures an SDRAM device for a specific mode of operation and specifies burst lengths for READ/WRITE and CAS latency. The load mode register command will be issued when the SDRAM controller is enabled and when the configuration changes via software.

The load mode register command is issued when all internal banks within the SDRAM device are idle. This occurs after the precharge.

3.4 Precharge/Load Mode Timing Example

An example of the initialization sequence for the SDRAM controller is given in Figure 1. The first cycle is a precharge. The assertion of CS, WE, and RAS, along with the appropriate address illustrates the precharge protocol.

Following the precharge is the delay required for idle state on all banks. The assertion of the previously mentioned signals, along with CAS and a configuration value placed on the address bus, completes the initialization cycle with a load mode register command.

4. SCHEMATIC ENTRY EXAMPLES

For your convenience, we have provided examples of the two most common configurations for SDRAM in an EP7312 implementation.

4.1 Two 16-bit devices

Figure 2 on page 5 illustrates the signal routing for the EP7312 controller and two SDRAM parts. This configuration uses a 32-bit data bus with two 16-bit wide SDRAM chips. The NEC part number for the parts used here is uPD4564163.

In this configuration, A15 is not required. It can be attached as a NC (no connect) or left floating. Row / column addressing does not require A15. A14 and A13 remain bank select pins. The lower 16 bits of data are controlled by SDQM[0:1]. The upper 16 bits by SDQM[2:3].

4.2 One 16-bit Device

For a 1x16 SDRAM configuration using a Micron MT48LC1M16A1S, the signal routing in Figure 3 on page 6 will work for this device. Micron has only two internal banks controlled by A11, which corresponds to our BA0 (A14).

Two byte masks for either 8 or 16-bit accesses are required as are the standard chip select, clocks and clock enable pins. Again, for this diagram, A16, A15 and A13 are not required as the SDRAM device has only 12 address lines, one address line being a bank select.

5. ADDITIONAL NOTES

5.1 Cache Enable for SDRAM Access

Unlike other SDRAM controllers, ours requires that cache be enabled for all SDRAM sections, pages, or small pages that are used as system memory. This is a requirement. When allocating memory for code, and task work-space, cache for these regions must be enabled. Any accesses from SDRAM regions that are not cache-enabled may

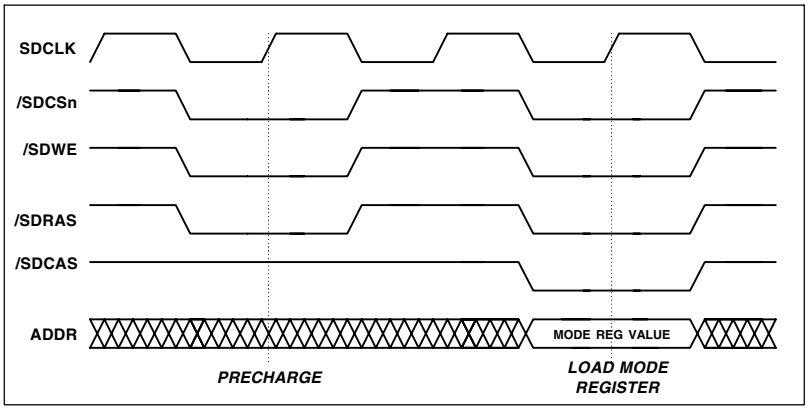

Figure 1. EP7312 SDRAM Initialization Sequence

result in corruption of the data stored in the SDRAM.

Enabling the cache for the SDRAM and other memory regions is beneficial. It results in a significant improvement in code execution time, up to a 10X performance increase. MMU configuration and programming is beyond the scope of this document. Please refer to the *ARM720T Technical Reference Manual* (available from ARM) for MMU programming information.

An example of the benefits of caching SDRAM is in using the SDRAM region as the LCD frame buffer. For the majority of designs, it is preferred to program the LCD DMA engine to access SDRAM. This region of memory will require that the cache be enabled.

5.2 Routing and Layout - Board Design

Layout for SDRAM should begin by placing the SDRAM devices as close to the processor as possible. SDCLK can be pushed out of phase. Loading of this pin in particular should be kept to a minimum. The SDRAM controller does allow for routing SDCLK to both the SDRAM devices and a test pin. Existing designs using the EP7312 typically route three devices to this bus successfully.

There are no design parameters for optimal trace distance and loading, but we have reference designs to illustrate this point. Isolation of SDCLK and control signals from high voltage and high frequency oscillators is highly recommended. As a rule of thumb, place and route SDRAM first when doing layout. Distances > 1.5 inches (38.1 mm) should be re-considered.

If loading on the address and data lines is going to exceed about 20 pf, consider buffering any additional peripherals that would access the address and data buses. This value is empirically based on existing designs.

The control pins, address and data do not have to be trace-length matched, though it would be preferred if possible. Since the maximum bus clock speed is 45 MHz when in a 90 MHz operating state, trace matching is less critical.

5.3 Tested Devices

NEC:

PD4564163G5

PD4516161A

Micron:

MT48LC4M16A2

Samsung

K4S281632D

6. CONCLUSION

The controller for the EP7312 is generic enough to support a wide range of SDRAM devices and across families of products. Schematics and additional information can be obtained from your local sales representative.

Your local FAE can assist you with selecting SDRAM devices for particular applications and program the controller accordingly. Additional information can be obtained by reading the JEDEC 2.1 standard for SDRAM initialization and configuration.

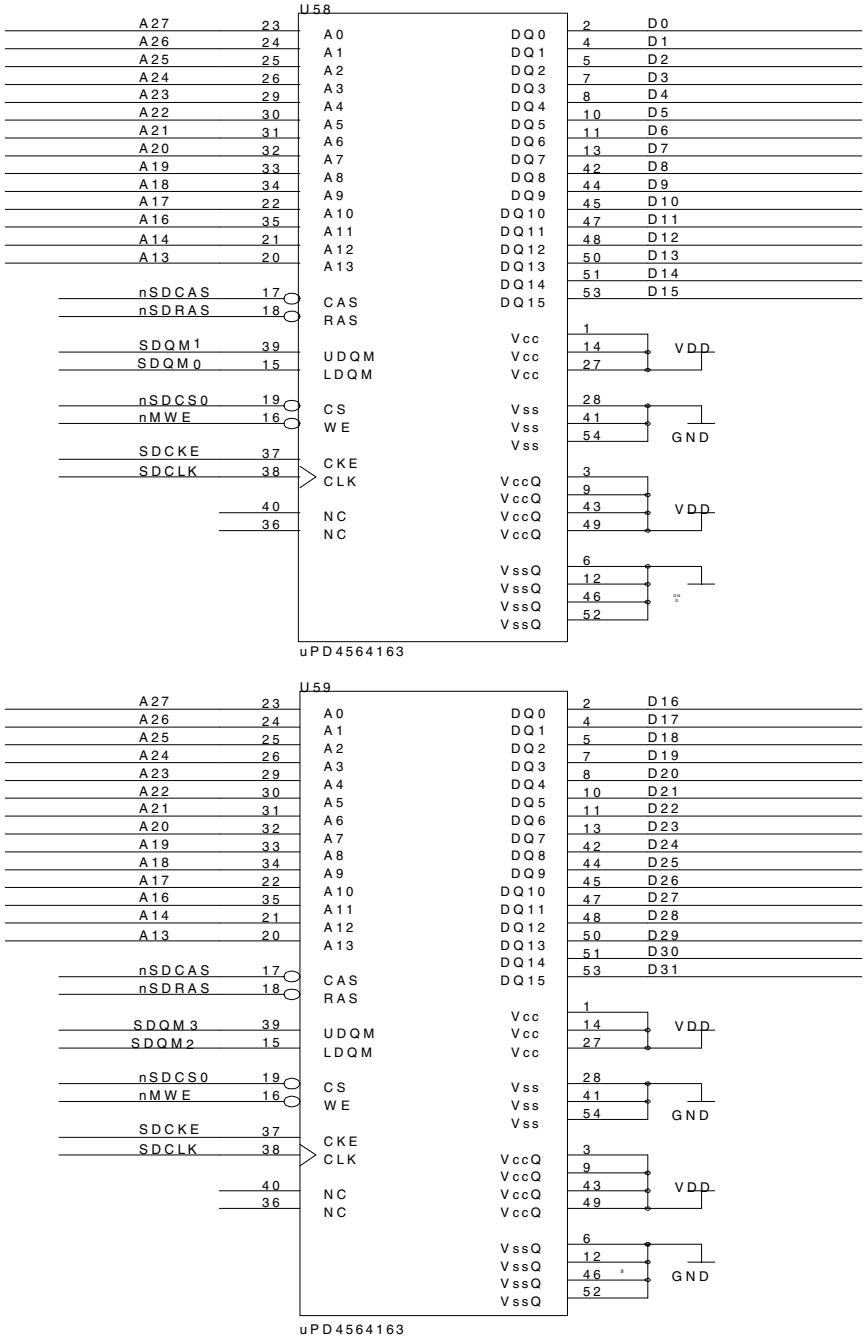

Figure 2. Two NEC uPD4564163 16-bit Devices

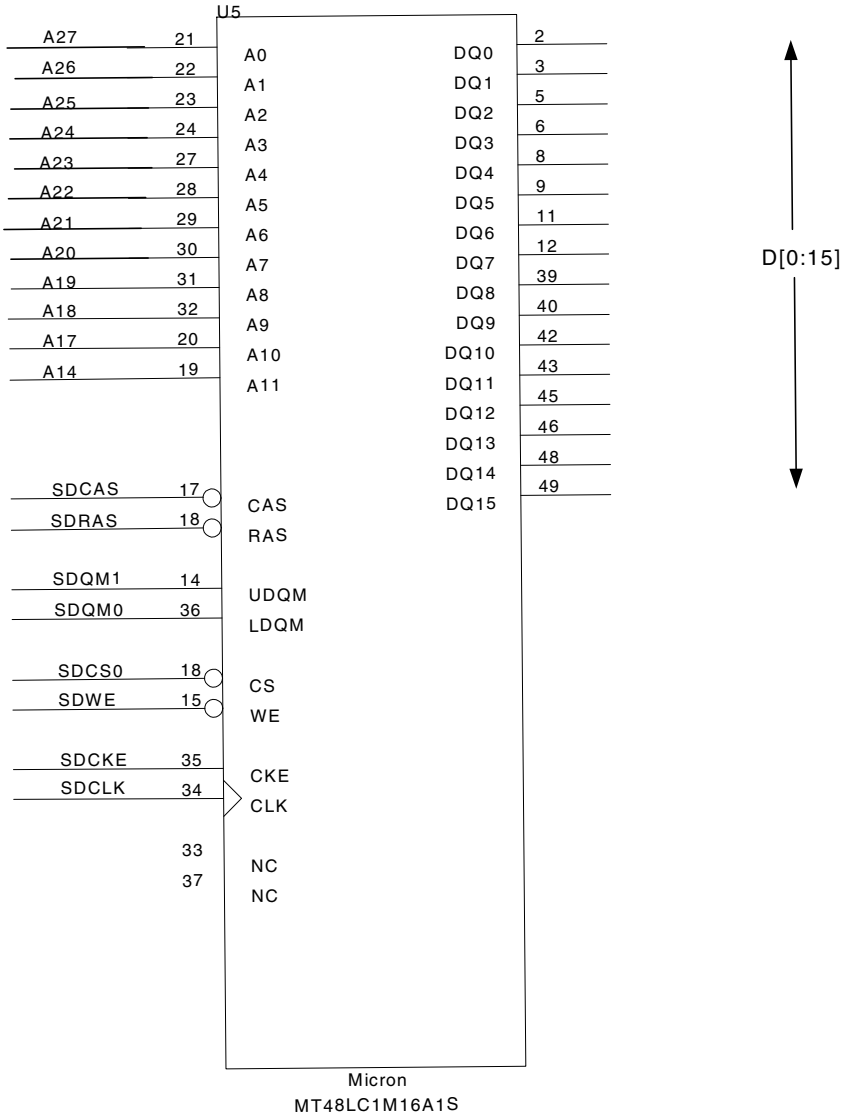

Figure 3. One Micron MT48LC1M16A1S 16-bit Device